Set	Items	Description
S1	2591327	CONFIGUR? OR SETTING? OR ARRANGE? OR SET()UP OR SETUP
S2	1569135	SELECT? OR MULTIPLEXER OR MUX
S3	5068740	SCAN? OR SEARCH? OR TEST OR SEEK? OR LOCAT? OR FIND? OR CONNECT? OR MATCH? OR INTERROGAT? OR EXAMIN? OR EVALUATE?
S4	3546884	(THREAD? OR STRING? OR CONNECT? OR CHAIN? OR LINE? OR ROW? OR TIER?)(2N)S3
S5	1933393	REGISTER OR MEMORY OR STORAGE OR BUFFER? OR CACHE? OR REPOSITORY OR IRM OR INFORMATION()RESOURCE()MANAGE????
S6	56504	(FIRST OR 1ST OR LEAD? OR PRIME OR PRIMAR OR INITIAL OR MAIN OR CARDINAL)(N)S5
S7	32697	(SECOND OR 2ND OR ANOTHER OR ADDITIONAL OR DIFFERENT)(N)S5
S8	2386735	ROUT??? OR FORWARD? OR SEND? ? OR DISPATCH? OR TRANSMIT? OR SHIP? OR TRANSFER?
S9	41584	(PARALLEL? OR MATCH? OR EQUAL? OR CORRESPOND?)(2N)(PATH OR LINE OR ROUTE)
S10	19488	(INPUT OR IN()PUT)()SIDE
S11	2818006	SWITCH? OR SWAP? OR CHANG? OR FLIP()FLOP OR EXCHANG?
S12	337505	(SOURCE OR ORIGIN? OR BEGIN? OR ROOT? OR FIRST OR 1ST OR PRIME OR PRIMARY OR INITIAL OR LEADING OR MAIN OR DOMINANT OR CARDINAL OR ORIGINAL)(2N)(PATH? OR LINK? ? OR CONNECT? OR LINE? ?)
S13	66425	(INPUT OR IN()PUT OR LOAD? OR INSERT? OR POST? OR PLACE? OR INCLUDE? OR INTEGRATE?)()(DATA OR INFORMATION)
S14	4338097	BETWEEN OR AMOUNG OR AMOUNGST OR AMID OR AMIDST
S15	71522	(NORMAL OR COMMON OR COMMONPLACE OR ORDINARY OR AVERAGE OR GENERAL OR USUAL? OR STANDARD)(2N)(PATH? OR LINK? ? OR CONNECT? OR LINE? ?)
S16	1016	(SELECTIVE? OR DISCRIMINATE? OR DISCRIMINATING OR DISCRIMINATIVE? OR DISCRIMINATORY)(N)(IDENTICAL OR MATCH? OR EXACT? OR SAME OR EQUAL OR CORRESPOND?)
S17	24317	S1 (3N) S2
S18	6138	S17 AND S4
S19	852	S1 AND S6 AND S4 AND S7
S20	0	S8 AND S9 AND S4 AND S10 AND S6 AND S7
S21	1	S2 AND S11 AND S12 AND S13 AND S14 AND S15 AND S9
S22	0	S9 AND S4 AND S10 AND S6 AND S7
S23	37	S17 AND S18 AND S19
S24	1	S14 AND S15 AND S16
S25	38	S23 OR S21
S26	1	S25 AND IC=G01R?
S27	38	S25 OR S26

File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200439
(c) 2004 Thomson Derwent

FAST & Focus

6/22/04

27/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07551342 **Image available**
SEMICONDUCTOR MEMORY

PUB. NO.: 2003-045182 [JP 2003045182 A]
PUBLISHED: February 14, 2003 (20030214)
INVENTOR(s): TANIZAKI HIROAKI
TOMISHIMA SHIGEKI
NIINOU MITSUTAKA
MARUTA MASANAO
KATO HIROSHI
ISHIKAWA MASATOSHI
TSUJI TAKAHARU
HIDAKA HIDETO
OISHI TSUKASA
APPLICANT(s): MITSUBISHI ELECTRIC CORP
MITSUBISHI ELECTRIC ENGINEERING CO LTD
APPL. NO.: 2001-233308 [JP 2001233308]
FILED: August 01, 2001 (20010801)
INTL CLASS: G11C-011/407; G11C-011/401

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor memory in which column system operation speed can be increased by equalizing loads of column selecting lines.

SOLUTION: First and **second memory** banks are provided with memory blocks of M pieces (M: even-numbers of 2 or more) having respectively a **first memory** region and a **second memory** region, and sense amplifier bands of M+1 pieces **arranged** at both sides of each memory block, first selecting lines for selecting the **first memory** region and second selecting lines for selecting the second region are **arranged**, the first **selecting lines** are **connected** to odd- numbered banks of the **first memory** banks and the sense amplifier bands of even-numbered banks of the **second memory** banks, the second selecting **lines** are **connected** to even-numbered banks of the **first memory** banks and the sense amplifier bands of odd-numbered banks of the **second memory** banks.

27/5/23 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008128809 **Image available**
WPI Acc No: 1990-015810/199003
XRPX Acc No: N90-012146
Integrated circuit card for computer - has special CPU storage area to hold either test program or applications program depending on which CPU wants
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: FUJIOKA S; FURUTA S; INOUE T; MATSUBARA T; TAKAHIRA K; YAMAGUCHI A
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3844032	A	19900104	DE 3844032	A	19881227	199003	B
FR 2633756	A	19900105				199008	
US 5019970	A	19910528	US 88276539	A	19881128	199124	
DE 3844032	C2	19940310	DE 3844032	A	19881227	199409	

Priority Applications (No Type Date): JP 88160746 A 19880630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3844032	A		13		
DE 3844032	C2		13	G06F-012/06	

Abstract (Basic): DE 3844032 A

The chip board has a first control device (13,14) to form a **first memory arrangement** in which at least a part of a first program (3) containing a test program is superimposed on a special area in the CPU's storage zone. This special area is accessible by using a command word shorter than those used for accessing the other areas. A second control device (19,21) forms a **second memory arrangement** in which a part of a **second memory** containing an applications program is superimposed on the special area.

A detector (22) recognises whether the CPU is executing a test or applications program. Changeover devices (18,20) actuate the first control devices when the CPU is to run a test and actuate the second control devices when the CPU is to run the applications program.

ADVANTAGE - Uses special area to execute test or applications program.

1/8

Title Terms: INTEGRATE; CIRCUIT; CARD; COMPUTER; SPECIAL; CPU; STORAGE; AREA; HOLD; TEST; PROGRAM; APPLY; PROGRAM; DEPEND; CPU
Derwent Class: T01; T04
International Patent Class (Main): G06F-012/06
International Patent Class (Additional): G06F-009/00; G06K-019/00
File Segment: EPI

27/5/29 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007201900
WPI Acc No: 1987-198909/198728
XRPX Acc No: N87-148846

Expandable electronic matrix for memory - has electronic elements of each matrix slice diagonally connected **to elements of adjacent matrix slice**

Patent Assignee: GTE COMMUNICATION SYSTEM CORP (SYLV)
Inventor: BURLINGAME C M
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4677436	A	19870630	US 84604762	A	19840427	198728	B
CA 1239700	A	19880726				198833	

Priority Applications (No Type Date): US 84604762 A 19840427
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4677436	A		7		

Abstract (Basic): US 4677436 A

The matrix of electronics element comprises a first matrix slice including a number of electronic elements **connected** serially to each other. A **first buffer** is **connected** to a source of matrix slice select signals and to a first element of the electronic elements **arranged** to **select** the first matrix slice responsive to a matrix slice select signal. A **second buffer** is **connected** to a source of element select signals and to the first electronic element **arranged** to **select** a first set of electronic elements responsive to an element select signal.

At least one additional matrix slice includes a number of electronic elements, a first electronic element of the first matrix slice diagonally **connected** to a second electronic element of the additional matrix slice, and each electronic element of the first matrix slide diagonally **connected** to a respective electronic element of the additional matrix slice in a similar manner as the first matrix slice first element. The last electronic element of the first matrix

slice diagonally **connected** to the first electronic element of the additional matrix slice.

1/4

Title Terms: EXPAND; ELECTRONIC; MATRIX; MEMORY; ELECTRONIC; ELEMENT; MATRIX; SLICE; DIAGONAL; **CONNECT** ; ELEMENT; ADJACENT; MATRIX; SLICE
Derwent Class: T01
International Patent Class (Additional): H04Q-001/00
File Segment: EPI

27/5/32 (Item 28 from file: 350)

007066515
WPI Acc No: 1987-066512/198710
XRPX Acc No: N87-050492

Digital processor control for computer - cyclically executes instructions from set and uses channel address register to store main memory **load**

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: FLECK R; JOHNSON W; KONG C; MOLLER O
Number of Countries: 012 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 213842	A	19870311	EP 86306267	A	19860814	198710	B
US 4734852	A	19880329	US 85771435	A	19850830	198816	
EP 213842	B1	19921021	EP 86306267	A	19860814	199243	
DE 3686991	G	19921126	DE 3686991	A	19860814	199249	
			EP 86306267	A	19860814		

Priority Applications (No Type Date): US 85771435 A 19850830
Cited Patents: 4.Jnl.Ref; A3...8917; FR 2151801; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 213842	A	E	15		
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
US 4734852	A		7		
EP 213842	B1	E	10	G06F-009/30	
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
DE 3686991	G			G06F-009/30	Based on patent EP 213842

Abstract (Basic): EP 213842 A

The control includes a file for storing plural-bit words each having a location designator, and a storage **connected** to a memory for temporarily receiving and storing a word retrieved from the memory. A circuit has a number of input terminals **connected** to the output terminals of the file and to the output terminal of the temporary storage for arithmetically combining selectable ones of the signals applied at the input terminals and for generating signals corresp. to the combination. Two further storages are **connected** to the file output terminals for temporarily receiving and storing signals corresp. to a word generated at these terminals and a fourth storage is provided to temporarily receive and store control information and to generate channel control signals.

A multiplexer is responsive to the signals from the combining circuit and the initial temporary storage to selectively conduct one of the signals to the file input terminal. The memory stores the contents of the one storage in response to the contents of two other storages and the combining circuit selects the contents of the **initial storage** until the multiplexer conducts the contents of this storage to the file.

USE/ADVANTAGE - Es.p for RISC computer. Performs data references to storage in parallel with instruction execution.

1/3

Title Terms: DIGITAL; PROCESSOR; CONTROL; COMPUTER; CYCLIC; EXECUTE; INSTRUCTION; SET; CHANNEL; ADDRESS; REGISTER; STORAGE; MAIN; MEMORY; LOAD
Index Terms/Additional Words: REDUCE; INSTRUCTION; SET; COMPUTER

Derwent Class: T01
International Patent Class (Main): G06F-009/30
International Patent Class (Additional): G06F-012/00
File Segment: EPI

```
Set     Items   Description
S1    1233582   CONFIGUR? OR SETTING? OR ARRANGE? OR SET()UP OR SETUP
S2     918714   SELECT? OR MULTIPLEXER OR MUX
S3    3807629   SCAN? OR SEARCH? OR TEST OR SEEK? OR LOCAT? OR FIND? OR CO-
          NNECT? OR MATCH? OR INTERROGAT? OR EXAMIN? OR EVALUATE?
S4    1012142   (THREAD? OR STRING? OR CONNECT? OR CHAIN? OR LINE? OR ROW?
          OR TIER?)(2N)S3
S5     831296   REGISTER OR MEMORY OR STORAGE OR BUFFER? OR CACHE? OR REPO-
          SITORY OR IRM OR INFORMATION()RESOURCE()MANAGE????
S6      15746   (FIRST OR 1ST OR LEAD? OR PRIME OR PRIMAR OR INITIAL OR MA-
          IN OR CARDINAL)(N)S5
S7      10119   (SECOND OR 2ND OR ANOTHER OR ADDITIONAL OR DIFFERENT)(N)S5
S8    2218490   ROUT??? OR FORWARD? OR SEND? ? OR DISPATCH? OR TRANSMIT? OR
           SHIP? OR TRANSFER?
S9       5341   (PARALLEL? OR MATCH? OR EQUAL? OR CORRESPOND?)(2N)(PATH OR
          LINE OR ROUTE)
S10       447   (INPUT OR IN()PUT)()SIDE
S11   2832429   SWITCH? OR SWAP? OR CHANG? OR FLIP()FLOP OR EXCHANG?
S12    103005   (SOURCE OR ORIGIN? OR BEGIN? OR ROOT? OR FIRST OR 1ST  OR -
          PRIME OR PRIMARY OR INITIAL OR LEADING OR MAIN OR DOMINANT OR
          CARDINAL OR ORIGINAL)(2N)(PATH? OR LINK? ? OR CONNECT? OR LIN-
          E? ?)
S13     53882   (INPUT OR IN()PUT OR LOAD? OR INSERT? OR POST? OR PLACE? OR
           INCLUDE? OR INTEGRATE?)()(DATA OR INFORMATION)
S14   2006253   BETWEEN OR AMOUNG OR AMOUNGST OR AMID OR AMIDST
S15     60685   (NORMAL OR COMMON OR COMMONPLACE OR ORDINARY OR AVERAGE OR
          GENERAL OR USUAL? OR STANDARD)(2N)(PATH? OR LINK? ? OR CONNEC-
          T? OR LINE? ?)
S16        97   (SELECTIVE? OR DISCRIMINATE? OR DISCRIMINATING OR DISCRIMI-
          NATIVE? OR DISCRIMINATORY)(N)(IDENTICAL OR MATCH? OR EXACT? OR
           SAME OR EQUAL OR CORRESPOND?)
S17      9983   S1 (3N) S2
S18       786   S17 (S) S4
S19         4   S1 (S) S6 (S) S4 (S) S7
S20         0   S8 (S) S9 (S) S4 (S) S10 (S) S6 (S) S7
S21         0   S2 (S) S11 (S) S12 (S) S13 (S) S14 (S) S15 (S) S9
S22         0   S9 (S) S4 (S) S10 (S) S6 (S) S7
S23         0   S17 (S) S18 (S) S19
S24         0   S14 (S) S15 (S) S16
S25       786   S17 (S) S18
S26        26   S25 (S) S15
S27         0   S25 (S) S16
S28         0   S17 (S) S16
S29        30   S19 OR S26
S30        27   S29 NOT PY>2001
S31        25   S29 NOT PD>20001009
S32        22   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/Jun 22
         (c) 2004 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/Jun W2
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 22
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/Jun W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 21
         (c) 2004 The Dialog Corp.
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 21
         (c) 2004 The Gale Group
```

32/3,K/3 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01170436 CMP ACCESSION NUMBER: EET19980824S0074
Chips mimic net-based storage
Fred Weniger, Director of FC Network Products Marketing, Vitesse Semiconductor Corp., Camarillo, Calif.
ELECTRONIC ENGINEERING TIMES, 1998, n 1022, PG82
PUBLICATION DATE: 980824
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Communications - Focus
WORD COUNT: 1624

... devices are, in addition to the SerDes, the port bypass circuit and the repeater/hub node.

A **common** configuration **connects** multiple systems with a high-performance JBOD ("just a bunch of disks") system. The host adapter is typically located in workstations, and servers are **connected** to the JBOD system through a hub with either copper or fiber-optic media. The hub allows systems to **connect** in a physical point-to-point star **configuration** . The hub **selectively** adds or drops devices from the loop , depending on whether they are sending valid data to the hub or not. The JBOD system **connects** multiple dual-channel disk drives with a common serial loop that is configured through port bypass circuits...

32/3,K/4 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01143639 CMP ACCESSION NUMBER: EET19971103S0002
Multifiber fiber-optic assemblies raise capabilities (Cover Feature)
Glenda Derman
ELECTRONIC ENGINEERING TIMES, 1997, n 979, PGP01
PUBLICATION DATE: 971103
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Product File
WORD COUNT: 1898

... Selections include MPX-to-MPX assemblies and MPX fanout assemblies that can incorporate non-MPX-terminated industry- **standard connectors** and combined fiber and copper solutions. Coupling adapters also are available.
Fiber-optic array connector systems from...

32/3,K/21 (Item 4 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

02875207 Supplier Number: 45835789 (USE FORMAT 7 FOR FULLTEXT)
PARALLEL-COMPUTING: HP ENTERPRISE PARALLEL-COMPUTING STRATEGY ADDRESSES HIGHEST-END DECISION-SUPPORT, OLTP NEEDS; HP ENTERPRISE PARALLEL SERVERS OFFER ONE OF TWO ROUTES TO PARALLEL PROCESSING
EDGE: Work-Group Computing Report, v6, n279, pN/A
Oct 2, 1995
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1276

... us well in our environment."
MULTIPLE CONFIGURATION SUPPORT
HP's Enterprise Parallel Computing strategy enables customers to

select the **configuration** that best suits their business and application needs. In a node-to-node "shared-nothing" configuration, each...

...disk and I/O storage. Alternatively, in a node-to-node "shared-everything" configuration, each node is **connected** to a **common** bank of arrayed disks.

Supporting multiple configurations is essential for the Enterprise Parallel Computing architecture to support...

```
Set     Items   Description
S1    1242265   CONFIGUR? OR SETTING? OR ARRANGE? OR SET()UP OR SETUP
S2    1256745   SELECT? OR MULTIPLEXER OR MUX
S3    6705710   SCAN? OR SEARCH? OR TEST OR SEEK? OR LOCAT? OR FIND? OR CO-
           NNECT? OR MATCH? OR INTERROGAT? OR EXAMIN? OR EVALUATE?
S4     819192   (THREAD? OR STRING? OR CONNECT? OR CHAIN? OR LINE? OR ROW?
           OR TIER?)(2N)S3
S5     976514   REGISTER OR MEMORY OR STORAGE OR BUFFER? OR CACHE? OR REPO-
           SITORY OR IRM OR INFORMATION()RESOURCE()MANAGE????
S6       8691   (FIRST OR 1ST OR LEAD? OR PRIME OR PRIMAR OR INITIAL OR MA-
           IN OR CARDINAL)(N)S5
S7       4506   (SECOND OR 2ND OR ANOTHER OR ADDITIONAL OR DIFFERENT)(N)S5
S8    2146829   ROUT??? OR FORWARD? OR SEND? ? OR DISPATCH? OR TRANSMIT? OR
            SHIP? OR TRANSFER?
S9      14223   (PARALLEL? OR MATCH? OR EQUAL? OR CORRESPOND?)(2N)(PATH OR
           LINE OR ROUTE)
S10       662   (INPUT OR IN()PUT)()SIDE
S11   2974433   SWITCH? OR SWAP? OR CHANG? OR FLIP()FLOP OR EXCHANG?
S12     64717   (SOURCE OR ORIGIN? OR BEGIN? OR ROOT? OR FIRST OR 1ST  OR -
           PRIME OR PRIMARY OR INITIAL OR LEADING OR MAIN OR DOMINANT OR
           CARDINAL OR ORIGINAL)(2N)(PATH? OR LINK? ? OR CONNECT? OR LIN-
           E? ?)
S13     48275   (INPUT OR IN()PUT OR LOAD? OR INSERT? OR POST? OR PLACE? OR
            INCLUDE? OR INTEGRATE?)()(DATA OR INFORMATION)
S14   4121770   BETWEEN OR AMOUNG OR AMOUNGST OR AMID OR AMIDST
S15     35883   (NORMAL OR COMMON OR COMMONPLACE OR ORDINARY OR AVERAGE OR
           GENERAL OR USUAL? OR STANDARD)(2N)(PATH? OR LINK? ? OR CONNEC-
           T? OR LINE? ?)
S16       167   (SELECTIVE? OR DISCRIMINATE? OR DISCRIMINATING OR DISCRIMI-
           NATIVE? OR DISCRIMINATORY)(N)(IDENTICAL OR MATCH? OR EXACT? OR
            SAME OR EQUAL OR CORRESPOND?)
S17      7975   S1 (3N) S2
S18       470   S17 AND S4
S19         3   S1 AND S6 AND S4 AND S7
S20         0   S8 AND S9 AND S4 AND S10 AND S7 AND S7
S21         0   S2 AND S11 AND S12 AND S13 AND S14 AND S15 AND S9
S22         0   S9 AND S4 AND S10 AND S6 AND S7
S23         0   S17 AND S18 AND S19
S24         0   S14 AND S15 AND S16
S25       470   S17 AND S18
S26        13   S25 AND S15
S27         0   S25 AND S16
S28        16   S19 OR S26
S29        14   S28 NOT PY>2001
S30        14   S29 NOT PD>20011009
S31        10   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/Jun W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jun W3
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Jun W2
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/May W5
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
```

31/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03614137 E.I. No: EIP93040761408
Title: Modeling of flow in heterogeneous reservoirs with Voronoi grid
Author: Palagi, C.L.; Ballin, P.R.; Aziz, Khalid
Corporate Source: Petrobras
Conference Title: Proceedings of the 12th SPE Symposium on Reservoir Simulation
Conference Location: New Orleans, LA, USA Conference Date: 19930228
E.I. Conference No.: 18188
Source: Proceedings of the SPE Symposium on Reservoir Simulation 1993. Publ by Soc of Petroleum Engineers of AIME, Richardson, TX, USA. p 291-299
Publication Year: 1993
CODEN: PSSREU
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 9306W1
Abstract: The flow rate at each interface between gridblocks is a function of an ?effective' permeability of the **connection** . The upscaling procedure consists of evaluating **average connection** permeabilities based on a smaller scale description of the reservoir. While several procedures have been reported in the literature to scale up permeability values for Cartesian grids, these procedures have not been extended to flexible grids. The Voronoi grid allows the specification of each gridpoint independently; therefore, it provides flexibility to represent wells and reservoir heterogeneities. This paper describes an upscaling procedure of permeability values at the interface of Voronoi gridblocks. The description of the heterogeneity, e.g., a stochastic image, is independent of the grid geometry. The power law average of the permeability values at each **connection** is computed automatically by the computer code. The optimum value of the power law coefficient is determined by comparing fine and coarse grid results for **selected** images and well **configurations** . Several well configurations were investigated with different grid geometries (Cartesian, hexagonal and locally refined hexagonal) using the same description of the reservoir. The optimum value of the power law coefficient was almost the same for all combinations of grid geometries and well configurations (between minus 0.5 and 0). Also several stochastically generated images of the reservoir, all honoring the same data, were analyzed. Again the optimum value of the power law coefficient was almost the same for all images. The hexagonal grid yields more robust results because each gridblock has more neighbors than the Cartesian grid. The use of local grid refinement around wells reduces the overall error. (Author abstract) 16 Refs.
Descriptors: *Flow of fluids; Mathematical models; Petroleum reservoirs; Oil wells
Identifiers: **Connection** permeabilities; Cartesian grids; Reservoir heterogeneities; Voronoi gridblocks; Power law coefficient
Classification Codes:
631.1 (Fluid Flow, General)
631 (Fluid Flow & Hydrodynamics); 921 (Applied Mathematics); 512 (Petroleum & Related Deposits)
63 (FLUID DYNAMICS & VACUUM TECHNOLOGY); 92 (ENGINEERING MATHEMATICS); 51 (PETROLEUM ENGINEERING)

31/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02794646 E.I. Monthly No: EIM8909-033003
Title: Sequoia approach to high-performance fault-tolerant I/O.
Author: Mark, Peter B.
Corporate Source: Sequoia Systems Inc, Marlboro, MA, USA
Conference Title: Compcon '89: Thirty-Fourth IEEE Computer Society

International Conference
Conference Location: San Francisco, CA, USA Conference Date: 19890227
E.I. Conference No.: 12357
Source: Digest of Papers - IEEE Computer Society International Conference. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2686-4), Piscataway, NJ, USA. p 565
Publication Year: 1989
CODEN: DCSIDU ISBN: 0-8186-1909-0
Language: English
Document Type: PA; (Conference Paper) Treatment: A; (Applications)
Journal Announcement: 8909
Abstract: Summary form only given. The Sequoia computer utilizes a modular, tightly-coupled multiprocessor architecture, with hardware fault detection and software fault recovery to achieve high degrees of reliability, availability, and data integrity. The computer comprises from one to 64 processor elements (PE), and from two to 128 memory elements (ME) and I/O processing elements (IOE). **Configurations** can be tailored to meet the needs of the aplications. Each processor element consists of two CPUs running in lockstep, with 256 kb of non-write-through cache. The non-write-through cache is the foundation of the fault-tolerant operation of the system. Each processor performs its work locally wihin its cache, periodically checkpointing its state to **main memory** . Each memory element consists of 16 Mb of memory, protected by ECC (error checking and correction), and 1024 test-and-set locks used to synchronize processor updates to shared data structures within the operating system. Writable data is shadowed in **main memory** ; the data is stored on two **different memory** elements. Each I/O processing element consists of CPUs running in lockstep, with 2 Mb of local memory. The I/O processors are **connected** to an IEEE-standard 796 bus the Multibus), which serves as an I/O bus **connecting** the IOE to up to 16 peripheral controllers of any type.
Descriptors: *COMPUTER SYSTEMS, DIGITAL--*Fault Tolerant Capability; COMPUTER ARCHITECTURE
Identifiers: SEQUOIA COMPUTER; HARDWARE FAULT DETECTION; SOFTWARE FAULT RECOVERY; ABSTRACT ONLY; TIGHTLY COUPLED MULTIPROCESSORS
Classification Codes:
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

31/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02552146 E.I. Monthly No: EIM8803-014690
Title: PERFORMANCE PREDICTIONS OF InSb SWITCHED FET HYBRID ARRAYS.
Author: Davis, R. Michael; Niblack, Curtiss A.
Corporate Source: Cincinnati Electronics Corp, Cincinnati, OH, USA
Conference Title: Instrumentation in Astronomy VI.
Conference Location: Tucson, AZ, USA Conference Date: 19860304
Sponsor: SPIE, Bellingham, WA, USA
E.I. Conference No.: 10824
Source: Proceedings of SPIE - The International Society for Optical Engineering v 627 pt 2. Publ by SPIE, Bellingham, WA, USA p 438-445
Publication Year: 1986
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-89252-662-9
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8803
Abstract: A technique, developed by Cincinnati Electronics and Jet Propulsion Laboratory, of utilizing charge integration with InSb photovoltaic arrays is described. This device uses a MOSFET switched silicon multiplexer to sequentially **connect** each detector to a **common line** and JFET amplifier. A noise model is presented which can be used to predict performance of the detector/multiplexer system. Performance prediction curves are included that allow comparisons and decisions related to system design. This noise model can be generalized to calculate

performance characteristics, particularly D* and NEP, for a detector/ **multiplexer configuration** . (Author abstract) 13 refs.
Descriptors: *TELESCOPES--*Infrared; PHOTOVOLTAIC CELLS; SEMICONDUCTOR DEVICES, FIELD EFFECT
Identifiers: CHARGE INTEGRATION; PHOTOVOLTAIC ARRAYS; SILICON MULTIPLEXER ; JFET AMPLIFIER; CAPACITIVE-DISCHARGE MODE (CDM)
Classification Codes:
741 (Optics & Optical Devices); 714 (Electronic Components); 941 (Acoustical & Optical Measuring Instruments)
74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS); 94 (INSTRUMENTS & MEASUREMENT)

31/5/9 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

00052464 INSPEC Abstract Number: C69008223
Title: Memory systems for using storage devices containing defective bits
Inventor(s): Sakalay, F.E.
Assignee(s): International Business Machines Corporation
Patent Number: US 3422402 Issue Date: 690114
Application Date: 651229
Priority Appl. Number: US 517264
Country of Publication: USA
Language: English Document Type: Patent (PT)
Abstract: A memory control system wherein memory devices containing defective elements or components are **arranged** to operate reliably. The system includes a **main memory** for storing a plurality of multibit data and a **first memory** address register for selecting address locations in the **main memory** . There are further provided a **second memory** address register with extra substitute address **locations connected** to the **main memory** , a large read only memory device having extra capacity with extra good address locations adapted to be substituted for address locations having defective bits, and an **arrangement** for directing an address with defective bits into a substitute position of the read only memory device and out to the **second memory** address register in the extra substitute address locations for changed and corrected interrogation of the **main memory** .
Subfile: C
Descriptors: storage units
Class Codes: C5320Z (Other digital storage)

31/5/10 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00300418 93UW01-005
Worldwide dial-up with the Worldblazer -- From Trailblazer to Worldblazer, Telebit's modems pick up speed
Granz, David
UNIX World , January 1, 1993 , v10 n1 p100-102, 3 Page(s)
ISSN: 0739-5922
Company Name: Telebit
Product Name: Worldblazer
Languages: English
Document Type: Hardware Review
Grade (of Product Reviewed): B
Geographic Location: United States
Presents a favorable review of Worldblazer ($1,099), a modem from Telebit Corp. of Sunnyvale, CA (800, 408). Says this high-speed modem provides fast and reliable communication over **standard** dial-up **lines** . Can **connect** to almost any other modem using industry-standard protocols. Its excellent transfer speed considerably reduces phone **connect** time. It is particularly good for UNIX-to-UNIX **connections** . Has a large number of features designed to support any requirements. Features several quick

setup parameter **selections** and some special purpose features, including a 10-number dialing directory, several ways to auto-dial a number, automatic callback-style security, and auto-timeout. Cautions that although the reference manuals are detailed, they are difficult to use. The ''why'' of the technical information is rarely explained. Says it is good for overseas calls due to its handling of flawed **connections** . Contains one photo. (vl)

Descriptors: Modem; Telecommunications; Hardware Review
Identifiers: Worldblazer; Telebit